REMARKS

The Applicants appreciate the Examiner's thorough examination of the subject application and the indication that claims 27-34 are in a condition for allowance and that claims 35-39, if rewritten, would be in a condition for allowance. Applicants request reconsideration of the subject application based on the following amendments and remarks.

Claims 1-39 are currently pending in the application. Claims 1, 7, 14, and 22 have been amended. Support for the amendments may be found throughout the specification. See, for example, the last line of page 17 to the first line of page 18. No new matter has been added by the amendments to the specification or the claims.

A brief description of the present invention may be of assistance in addressing the rejections set forth by the Examiner under §102 and §103.

The present invention provides an active matrix substrate, comprising:

electrode wires constituted by scanning electrode wiring and signal electrode wiring that are arranged in a lattice;

an insulating film provided at least on the electrode wires so as to have openings in predetermined areas at least on either the scanning electrode wiring or on the signal electrode wiring; and

a metal layer in the openings of the insulating film and in contact with the electrode wiring to cap the openings.

That is, claims 1, 7, 14, and 22, as amended, provide active matrix substrates in which a metal layer (12) is selectively stacked on the electrode wiring, e.g., scanning electrode wiring (2) and signal electrode wiring (6), in holes of the insulating film (8). Thus, looking at Figure 2(e), the metal layer (12) is situated within the hole of the insulating film (8) and is in direct contact with signal electrode wiring (6) and the scanning electrode wiring (7). Moreover, the metal layer formed in the holes of the insulating film such that the metal layer caps the openings in the

insulating layer. See, for example, the specification at page 18, line 12 to page 19, line 3; or more particularly, page 18, line23 to page 19, line 3 and Figure 2 of the instant application.

A protective insulating film (13) is then deposited over the insulating film (8) and may further be deposited over one or more of the metal layers formed in the holes of the insulating film (for example signal electrode wiring (6) of Figure 2). Other metal layers are coated by at least a portion of a pixel electrode (15)fabricated from a conductive transparent metal oxide.

Claims 1, 5, 7, 11, 12, 22, and 23 were rejected under 35 U.S.C. §102(e) as being allegedly anticipated by Hirabayashi et al. (U.S. Patent 6,375,544).

Claims 2-4, 9, 8-10, 13-21, and 24-26 were rejected under 35 U.S.C. §103(a) as being allegedly unpatentable over Hirabayashi as applied to claims 1, 5, 7, 11, 12, 22, and 23.

For the sake of brevity, the two § 102 and § 103 rejections are addressed in combination. Such a combined response is considered appropriate because *inter alia* each of the rejections relies on the Hirabayashi patent as the sole or primary citation.

Each of the rejections is traversed.

As the rejections are understood, the Office Action relies on the assertion that the structure of Hirabayashi depicted in Figure 2 provides a metal layer (15) stacked on an electrode wiring (10) in the contact hole (16) formed in a gap (12b) of a second metal layer (12) is structurally equivalent of the instantly claimed invention as the basis for the rejection of the claims under §102 and §103.

This assertion does not appear to be correct.

As the reference is understood, Hirabayashi teaches metal plugs deposited in holes present in laminated structure having both insulating and conductive layers. That is, metal plug

15 is formed in a hole formed in a laminate structure comprising a metal conductive layer interposed between two insulating layers. Thus, Hirabayashi describes a liquid crystal panel substrate including a shading film 12 composed of a second metal layer, a second interlayer insulation film 11 under the shading film 12, a wiring film 10 composed of a first metal layer under the second interlayer insulation film, a pixel electrode composed of a third metal layer on a third interlayer insulation film 13 on the shading film 12, and a connecting plug 15 connecting the wiring film 10 and the pixel electrode through the opening provided in the shading film 12.

Moreover, *Hirabayashi* teaches an electro-optical device substrate, such as a liquid crystal panel substrate, having a layered film structure of a plurality of interlayer insulation films and a plurality of conductive layers alternately formed in a pixel region formed on a substrate, wherein the electro-optical device substrate has a structure requiring no additional deposition step and having a uniform polishing rate for the interlayer insulation film without thickening of the interlayer insulation film.

Further, *Hirabayashi* is aimed at providing an electro-optical device substrate, which has a flattened polished surface of the interlayer insulation film in the scaling region as well as in the pixel region, an improved reflectance of the pixel electrode, and which permits ready scaling agent, and an optimized etching time of the contact hole. See, for example, column 6, lines 1-17 of Hirabayashi.

More specifically, the connection plug 15 composed of a high-melting-point metal connects the relay wiring 10 and the pixel electrode 14, skipping one metal layer of the shading layer 12. See, column 14. lines 52-55 of Hirabayashi. Therefore, Hirabayashi fails to teach or suggest an active matrix substrate having a meal layer formed on an electrode wire in an opening provided in an insulating layer thereby "capping" the insulating layer openings.

In contrast, the present invention provides active matrix substrate having an insulating film having openings at least either on the scanning electrode wiring or on the signal electrode wiring, and a metal layer in the openings of the insulating film and in contact with the electrode

wiring, and also the manufacturing method thereof, a display device and an image-capturing device using the substrate.

Further, the present invention provides active matrix substrates and methods of making same which reduce the amount of metal wasted during fabrication, reduce the resistance of electrode wires, and thereby attempting to increase the display area and precision of the flat panel display, the flay panel sensor, etc., that is, to offer an active matrix substrate that is suitably used in these devices and also offer a method of manufacturing such an active matrix substrate, and also offering a display device and an image-capturing device incorporating the substrate . See, for example, page 4, last line to page 5, line 13 of the instant specification.

Therefore, the present invention provides a structure in which a metal layer is selectively formed on the electrodes in the openings that are cut out of the insulating film. Thus, the active matrix substrate of the invention are prepared without the conventional step of etching a deposited metal layer in a predetermined pattern to generate the desired metal line pattern. See, page 8, line 20 to page 9, line 6 of the instant specification.

More specifically, the openings (11a) are provided on the other portions of the source electrode that the extended portions where the TFT elements are provided (See Figure 2), and the metal layer is formed on the source electrode 6 and the drain electrode 7 to cap the openings 11a and 11b (See, page 17, line 24 to page 18, line 1 of the instant specification), and the metal layer formed on the source electrodes 6 is covered with the interlayer insulating film 13, as well as the insulating protection film 8, and is therefore protected by the interlayer insulating film 13 (see page 22, lines 20-24 of the instant specification).

Thus Hirabayashi teaches a relay wiring 10 in contact with the drain region 5b through the contact hole 6b, and a connecting plug 15 in contact with the relay wiring 10 and the pixel electrode 14. However, Hirabayashi teaches the connecting plug is disposed in a connecting hole 16 of a laminated structure having insulating and conductive layers. Thus, Hirabayashi fails to teach a semiconductor structure in which the connecting plug 15 is disposed in an opening of an

insulating film. See, Figure 2 of Hirabayashi and particularly the arrangement of components 10, 11, 12, 12a, 13, 15, and 16.

Please also not that, in the Hirabayashi structure, a shading film 12 made of a second metal layer is provided between the second interlayer insulating film 11 and the third interlayer film 13, and the opening is formed 12a in which the connecting plug 15 is disposed is an opening in the shading film 12. Such a structure is different from the metal layer of the present invention, which is covered by the interlayer insulating film 13 or a pixel electrode 15 (composed of a transparent conductive metal oxide).

For at least the reasons discussed herein, Hirabayashi fails to teach or suggest the active matrix substrates of the claimed invention.

Thus claims 1, 7, 14, and 22 are patentable Hirabayashi. Claims 2-6, 8-13, 15-21, and 23-26 depend from one of claims 1, 7, 14, or 22 and are therefore also patentable over Hirabayashi.

Although it is not believed that any additional fees are needed to consider this submission, the Examiner is hereby authorized to charge our deposit account no. 04-1105 should any fee be deemed necessary.

Respectfully submitted,

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John B. Alexander (Reg. No. 48,399)
EDWARDS & ANGELL, LLP
Dike, Bronstein, Roberts & Cushman
Intellectual Property Practice Group
P. O. Box 9169
Boston, MA 02209
Tel: (617) 439-4444
Fax: (617) 439-4170 / 7748

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